IN THE CLAIMS

1. (Currently amended) A semiconductor wafer comprising:

a top surface, a bottom planar surface, and an outwardly convex edge surface connecting the top surface and the bottom planar surface, the outwardly convex edge surface having an upper side surface and a lower side surface;

a boundary between the bottom planar surface and the outwardly convex edge surface; and

a marking region disposed on the lower side surface, wherein a wafer identification indication is carved in the marking region,

wherein a distance from a center of the bottom planar surface to a first portion of the boundary adjacent to the marking region is less than a distance from the center of the bottom planar surface to a second portion of the boundary.

2-4. (Cancelled)

5. (Previously presented) The semiconductor wafer of claim 1, wherein a width of a portion of the lower side surface adjacent to the second portion of the boundary is the same as a width of the upper side surface.

6. (Previously presented) The semiconductor wafer of claim 1, wherein a thickness of the upper side surface is thinner than a thickness of a region on the lower side surface.

7. (Previously presented) The semiconductor wafer of claim 1, wherein the lower side surface is thicker than the upper side surface along an entire circumference of the semiconductor wafer.

8. (Original) The semiconductor wafer of claim 1, wherein the wafer identification indication comprises dots that are formed by a laser beam.

9. (Original) The semiconductor wafer of claim 1, wherein the wafer identification indication comprises patterns representing information.

10. (Cancelled)

11. (Currently amended) A semiconductor wafer comprising:

a planar bottom surface;

an outwardly curved edge surface, the outwardly curved edge surface having an upper side surface and a lower side surface; and

a boundary between the planar bottom surface and the lower side surface;

a marking region disposed on the lower side surface, wherein a wafer identification indication is carved in the marking region, and wherein the outwardly curved edge surface is asymmetric with respect to the upper and the lower side surfaces, and wherein a distance from a center of the planar bottom surface to a first portion of the boundary adjacent to the marking region is less than a distance from the center of the planar bottom surface to a second portion of the boundary.

12. (Previously presented) The semiconductor wafer of claim 11, wherein a width of the upper side surface equals a width of the lower side surface.

13 (Previously presented) The semiconductor wafer of claim 11, wherein a width of the upper side surface does not equal a width of the lower side surface.

14. (Previously presented) The semiconductor wafer of claim 11 wherein the marking region includes indentations that identify the wafer.

15-21. (Cancelled)

22. (Previously presented) The semiconductor wafer of claim 1, wherein the outwardly convex edge surface is asymmetric with respect to the upper and the lower side surfaces.

23. (Previously presented) The semiconductor wafer of claim 1, wherein the top surface is planar and a radius of a boundary between the top surface and the outwardly convex edge surface is constant.

24. (Previously presented) The semiconductor wafer of claim 11, further comprising a planar top surface, wherein a radius of a boundary between the planar top surface and the outwardly convex edge surface is constant.

25. (Currently amended) A semiconductor wafer comprising:

a top surface, a bottom planar surface, and an outwardly convex edge surface connecting the top surface and the bottom planar surface, the outwardly convex edge surface having an upper side surface and a lower side surface;

a substantially circular boundary between the bottom planar surface and the outwardly convex edge surface;

a marking region disposed on the lower side surface; and

a wafer identification indication carved in the marking region,

wherein a distance from a center of the bottom planar surface to a first portion of the boundary adjacent to the marking region is less than a distance from the center of the bottom planar surface to a second portion of the boundary.

26-28. (Cancelled)

29. (Previously presented) A semiconductor wafer comprising:

a top surface, a bottom surface, and an outwardly convex edge surface connecting the top surface and the bottom surface and defining an outer perimeter of the semiconductor wafer, the outwardly convex edge surface comprising:

an upper side surface; and

a lower side surface;

a boundary between the bottom surface and the lower side surface, wherein a width of a first portion of the lower side surface extending contiguously between a first portion of the outer perimeter and a first portion of the boundary is greater than a width of a second portion of the lower side surface extending contiguously between a second portion of the outer perimeter and a second portion of the boundary;

a marking region in the first portion of the lower side surface; and

a wafer identification indication in the marking region.

30. (Currently amended) A semiconductor wafer comprising:

a top surface, a bottom surface, and an outwardly convex edge surface connecting the top surface and the bottom surface and defining an outer perimeter of the semiconductor wafer;

a boundary between the bottom surface and the outwardly convex edge surface, wherein a distance between a first portion of the boundary and a first portion of the outer perimeter is greater than a distance between a second portion of the boundary and a second portion of the ~~boundary~~ outer perimeter;

a marking region on the outwardly convex edge surface between the first portion of the boundary and the first portion of the outer perimeter; and

a wafer identification indication in the marking region.

31. (Currently amended) A semiconductor wafer comprising:

a top surface, a planar bottom surface, and an outwardly convex edge surface connecting the top surface and the planar bottom surface;

a boundary between the planar bottom surface and the outwardly convex edge surface, wherein a first portion of the boundary has a first curvature within the plane of the planar bottom surface and a second portion of the boundary has a second curvature within the plane of the planar bottom surface greater than the first curvature;

a marking region on a portion of the outwardly convex edge surface adjacent to the first portion of the boundary; and

a wafer identification indication in the marking region.